

## FEATURES

- TI TMS320C6454 Digital Signal Processor
  - 720 MHz (1 GHz option)
  - 1 MB cache (2 MB option)
  - Integrated 10/100/1000 EMAC
  - 2 Integrated McBSPs
  - JTAG Emulation/Debug
- On-Board Xilinx FPGA
  - XC3S2000 (XC3S4000 option)
  - 300 MHz Clock Logic
  - 720 KBits Block RAM
  - 20,480 Slices
  - JTAG Interface/Debug
- On-Board 10/100 Ethernet PHY
- 128 MB CPU DDR-2 SDRAM
- 64 MB FPGA DDR SDRAM
- 16 MB NOR FLASH
- Standard SO-DIMM-200 Interface
  - 140 FPGA User I/O Pins
  - 2 McBSP Interfaces
  - I2C Interface
  - 10/100 Ethernet Interface
  - 3.3 V Power Interface
- Expansion I/O Connector
  - DSP Rapid IO Interface
  - DSP PCI I/O Interface

## APPLICATIONS

- Embedded Instrumentation
- Rapid Development / Deployment
- Embedded Digital Signal Processing
- Real-time Audio / Video Processing



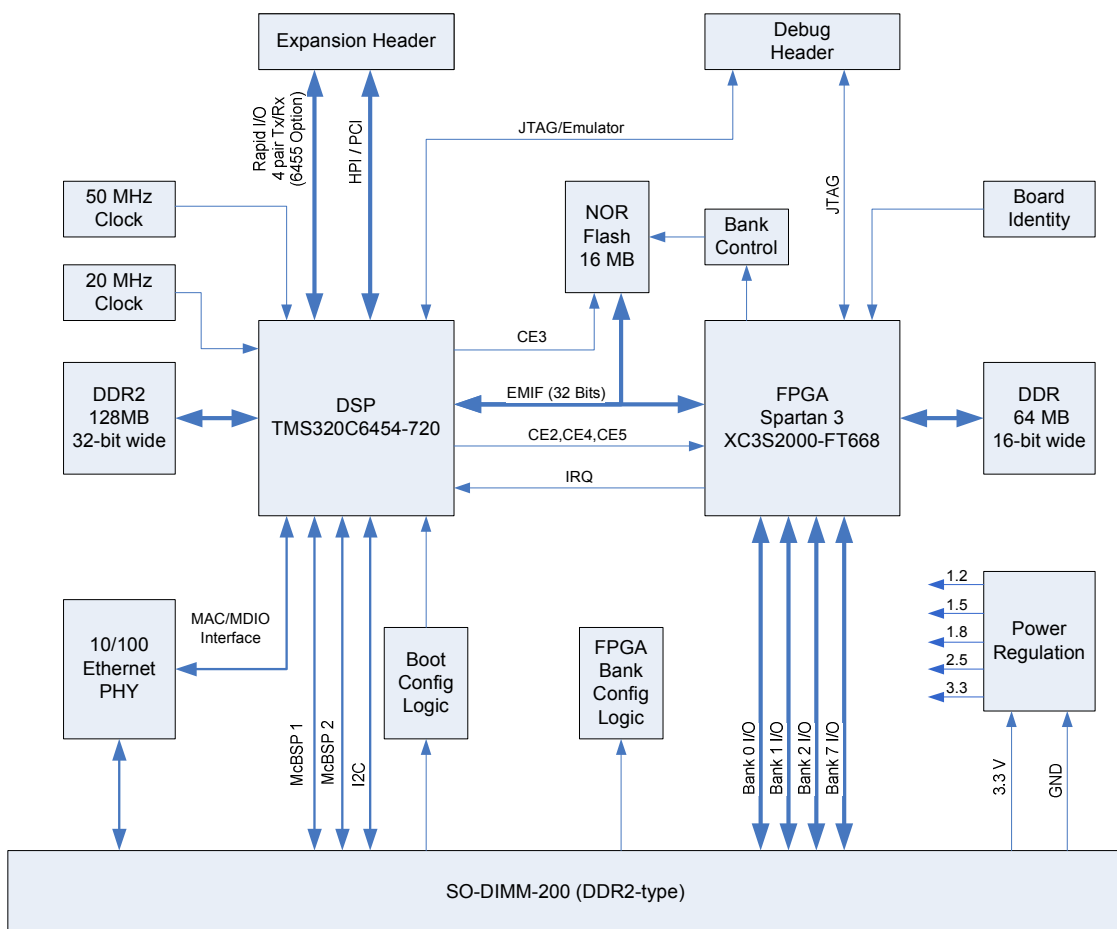
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## DESCRIPTION

The MityDSP-Pro is a highly configurable, high performance, small form-factor processor card that features a Texas Instruments TMS320C6454 720 MHz Digital Signal Processor (DSP) tightly integrated with a Xilinx XC3S2000 Spartan Field Programmable Gate Array (FPGA), FLASH and DDR SDRAM memory subsystems. Both the DSP and the FPGA are capable of loading/executing programs and logic images developed by end users. The MityDSP-Pro provides a complete digital processing infrastructure necessary for embedded applications development.

Users of the MityDSP-Pro are encouraged to develop applications and FPGA firmware using the MityDSP hardware and software development kit provided by Critical Link LLC. The development kit includes API libraries compatible with the TI Code Composer Studio compiler as well as FPGA netlist components compatible with the Xilinx ISE FPGA synthesis tool. The libraries provide the necessary functions needed to configure the MityDSP-Pro, program standalone MityDSP embedded applications, and interface with the various hardware components on the board. In addition, the libraries include several interface “cores” – FPGA and DSP software modules designed to interface with various data converter modules (ADCs, DACs, LCD interfaces, etc) – as well as bootloading and FLASH programming utilities.

Figure 1 provides a top level block diagram of the MityDSP-Pro processor card. As shown in the figure, the primary interface to the MityDSP-Pro is through a standard DDR2 type SO-DIMM-200 card edge interface. The interface provides 3.3 V power, configuration control, Ethernet connectivity, inter-integrated circuit (I2C) connectivity, synchronous serial connectivity, and 140 pins of configurable FPGA I/O for application defined interfacing. Details of the SO-DIMM connector interface are included in the SO-DIMM-200 Interface Description, below.



**Figure 1 MityDSP-Pro Block Diagram**

### FPGA Bank I/O

The MityDSP2 provides 140 lines of FPGA I/O directly to the SO-DIMM-200 card edge interface. The 140 lines of FPGA I/O are distributed across 4 banks of the FPGA. These I/O lines and their associated logic are completely configurable within the FPGA.

With the Xilinx Spartan series of FPGA, each bank may be configured to operate on a different electrical interface standard based on input voltage and termination configurations. The MityDSP-Pro provides, for each of the externally accessible FPGA banks, a configuration block to allow selection of the following voltage and termination standards:

- 2.5 V LVDS with 100 Ohm DCI termination
- 2.5 V LVDS with no DCI termination
- 3.3 V CMOS (pull-up / pull-down / floating configurable per pin)
- 2.5 V CMOS (pull-up / pull-down / floating configurable per pin)

For complete details regarding hardware bank voltage configuration please refer to the SO-DIMM-200 Interface description and the appropriate Spartan-3 manuals from Xilinx.

### **Integrated DSP Communications Modules**

The C6454 processor includes several on-chip communications modules. The MityDSP-Pro design provides access to the several of the modules through the SO-DIMM-200 card edge interface.

The Ethernet MAC/MDIO interface on the DSP has been integrated with an on-board Ethernet PHY device. The output (TTL) signals of the PHY device are brought to the SO-DIMM-200 connector. In order to leverage the Ethernet interface, application cards need only supply the pulse magnetics transformer and the final RJ-45 ethernet style connector. The MityDSP software developer's kit includes a software driver and port of the LwIP TCP/IP protocol stack for use with the Ethernet interface.

The inter-integrated circuit (I2C) signals have been routed directly from the DSP part to the SO-DIMM-200 interface. TI provides several I2C interface libraries for integration with various data acquisition modules. In addition, the I2C interface may be used to boot the DSP processor (see the SO-DIMM-200 interface description for details on MityDSP-Pro boot configuration).

The DSP also includes two multichannel buffered serial ports (McBSPs) which have been routed directly to the SO-DIMM-200 interface. Both Critical Link (as part of the MityDSP development kit) and TI provide several McBSP interface libraries for integration with various data acquisition modules.

### **EMIF Interface**

The C6454 DSP and the Spartan FPGA are connected using the DSP External Memory Interface (EMIFA). The EMIFA interface includes 4 chip select spaces. The EMIFA interface supports multiple data width transfers and bus wait state configurations based on chip select space. 8, 16, 32 bit data word sizes may be used. Three of the four chip select lines are reserved for the FPGA interface. The MityDSP-Pro also includes lines between the FPGA and the MityDSP for the purposes of generating interrupt signals.

In addition to the FPGA, 16 MB of on-board NOR FLASH memory is also connected to the DSP using the EMIF. The FLASH memory is connected to fourth chip select line of the EMIF (CE3). The FLASH memory is typically used to store the following types of data:

- secondary bootloader DSP software
- FPGA bootloader images
- application DSP software
- application FPGA images
- application data (non-volatile storage)

The DSP EMIF interface is only capable of addressing 4 MB of data on the EMIF interface. In order to provide access to the remaining 12 MB of FLASH memory, the upper address lines of the FLASH are controlled by Bank Control logic. Upon reset the Bank Control Logic defaults to bank zero for bootloading support. Following bootloading, the bank control logic is controlled by the FPGA. Refer to the MityDSP User's Guide for more information on bank control logic.

### **System Memory**

The C6454 includes 32 KB internal level 1 (L1) cache and 1 MB internal SRAM that may be used as SRAM or level 2 (L2) cache for application data and code during runtime. The C6455 option includes a 2 MB internal SRAM. For additional DSP software program and runtime data storage, a dedicated 128 MB of DDR2 memory is available via the DDR2 control interface on the DSP. The memory is 32 bits wide and is capable of running at 200 MHz providing a burst throughput of 1.6 GB per second to the processor.

For the FPGA, a separate 64 MB of DDR (type 1) memory is provided. The memory interface is 16 bits wide and is capable of running at 100 MHz providing a burst throughput of 400 MB per second to the FPGA. Common uses for the FPGA memory include custom data collection systems, video frame buffers, and MicroBlaze program storage.

### **Debug Interface**

Both the JTAG interface signals for the FPGA and the JTAG and emulator signals for the C6454 processor have been brought out to a connector/header for use with in-circuit debugging. The JTAG chains are separate on the interface. With an appropriate break-out cable, the interface will support the use of standard Xilinx Platform JTAG cable programming and the Spectrum Digital processor emulator (or equivalent). Details of the pin-outs for the debug header are included in the Debug Interface Description, below.

### **Expansion Interface**

For system expansion, the MityDSP2 also provides a low profile Hirose FX8-TBD-TBD connector interface that may be used to access the Host-Port-Interface (HPI) or the Peripheral-Control-Interconnect (PCI) ports of the C6454 bus. In addition, pads for four

lanes of transmit and receive Rapid I/O data lines (and associated clocks) which are found on the TI TMS320C6455 processor (option) are also provided.

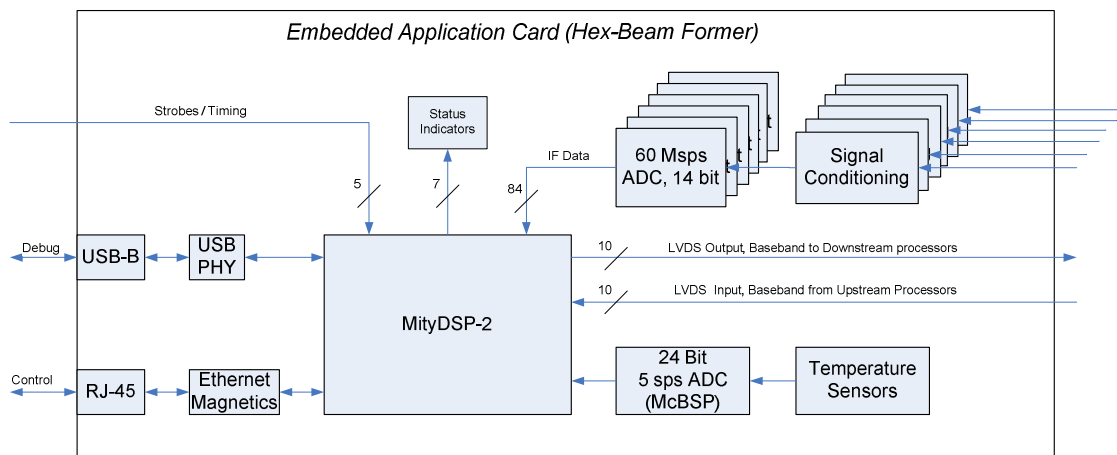
**Growth Options**

The MityDSP-Pro has been designed to support several upgrade options listed in the table below. For ordering information and details regarding these options, please contact a Critical Link sales representative.

CPU Options	Description
TMS320C6454-720	720 MHz Commercial DSP
TMS320C6454-1000	1 GHz core clock CPU speed.
TMS320C6455-720	Base Offering, 720 MHz core clock CPU speed, includes Rapid I/O expansion and 2 MB On-Chip L2 SRAM / Cache
TMS320C6455-1000	1 GHz core clock CPU speed, includes Rapid I/O expansion and 2 MB On-Chip L2 SRAM / Cache
FPGA Options	Description
XC3S1500-FT676*	13,312 Slices, 576 Kbits Block RAM
XC3S2000-FT676*	Base Offering, 20,480 Slices, 720 Kbits Block RAM
XC3S4000-FT676*	27,648 Slices, 1,728 Kbits Block RAM
*please contact Critical Link for information regarding specific speed grades	

**Example Application**

The figure below illustrates an example application utilizing the MityDSP-Pro processor card. The example application is a 6 way signal beamformer for use in a radar system. The card is required to capture 6 channels of IF signal data, downconvert the data to baseband, sum the signals together with the input channels and data provided from upstream processors, and send the results to downstream processing.



**Figure 2 Typical MityDSP-Pro Application**

In the example application, a designer leverages three of the 4 FPGA I/O banks as 3.3 V CMOS interface and is able to integrate 6 14 bit ADC circuits directly to the MityDSP-Pro FPGA as well as various strobe signals and status indicators. The fourth bank is

reserved for LVDS signaling and is used to receive and transmit data from upstream and downstream processors.

The user is able to utilize the McBSP interface of the MityDSP-Pro to capture on-board temperature data for health monitoring. In addition, the Ethernet interface and a USB interface is added to provide debug and status and control information to external control units.

Within the MityDSP-Pro, the user is able to utilize the FPGA multiply accumulator engines and programmable logic to capture, baseband, and integrate each of the ADC channels on the main board. The TI processor can be used to compute complex coefficients used in the beamforming process and provide the command and control interface for the entire card.

With the application, the user needs only focus on the details of the application specific problems at hand: e.g., developing the appropriate signal conditioning and application software and firmware. The framework for the processing and interconnects is completely designed with the integration of the MityDSP2.

## ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage, Vcc            3.4 V

Storage Temperature Range            -65 to 80C

Shock, Z-Axis                                ±10 g

Shock, X/Y-Axis                            ±10 g

## OPERATING CONDITIONS

Ambient Temperature                    0 to 55C  
Range

Humidity                                    0 to 95%  
Non-  
condensing

Vibration, Z-Axis                         TBS

Vibration, X/Y-Axis                      TBS

## SO-DIMM-200 Interface Description

The primary interface connector for the MityDSP-Pro is the SO-DIMM-200 card edge interface.

**Table 1 SO-DIMM-200 Pin-Out**

Pin	Signal	FPGA Bank	Pin	Signal
1	3.3 V	-	2	3.3 V
3	3.3 V	-	4	3.3 V
5	3.3 V	-	6	3.3 V
7	GND	-	8	GND
9	GND	-	10	GND
11	MRESET#	-	12	BOOT_MODE
13	ETH_TD_P	-	14	RS232_TXD
15	ETH_TD_N	-	16	RS232_RXD
17	ETH_RD_P	-	18	RS232_RTS
19	ETH_RD_N	-	20	RS232_CTS
21	FPGA_RSV1	-	22	SCL
23	FPGA_RSV2	-	24	SDA
25	CLKR0	-	26	CLKR1
27	CLKX0	-	28	CLKX1
29	DR0	-	30	DR1
31	DX0	-	32	DX1
33	FSR0	-	34	FSR1
35	FSX0	-	36	FSX1
37	VCCO_2	-	38	VCCO_1
39	VCCO_0	-	40	VCCO_7
41	GND	2	42	GND
43	ODD1_P.N26	2	44	EVN1_P.N22
45	ODD1_N.N25	2	46	EVN1_N.N21
47	ODD2_P.M26	2	48	EVN2_P.N24
49	ODD2_N.M25	2	50	EVN2_N.N23
51	ODD3_P.M22	2	52	EVN3_P.M24
53	ODD3_N.M21	2	54	EVN3_N.L23
55	ODD4_P.L26	2	56	EVN4_P.K24
57	ODD4_N.L25	2	58	EVN4_N.K23
59	ODD5_P.K26	2	60	EVN5_P.J25
61	ODD5_N.K25	2	62	EVN5_N.J24
63	GND	2	64	GND
65	ODD6_P.K22	2	66	EVN6_P.H24
67	ODD6_N.K21	2	68	EVN6_N.H23
69	ODD7_P.H26	2	70	EVN7_P.J23
71	ODD7_N.H25	2	72	EVN7_N.J22
73	ODD8_P.J21	2	74	EVN8_P.H21
75	ODD8_N.H22	2	76	EVN8_N.H20
77	ODD9_P.D26	2	78	EVN9_P.E24
79	ODD9_N.D25	2	80	EVN9_N.E23
81	ODD10_P.F21	1	82	EVN10_P.C23
83	ODD10_N.E21	1	84	EVN10_N.B23
85	GND	1	86	GND
87	ODD11_P.E20	1	88	EVN11_P.C22
89	ODD11_N.D20	1	90	EVN11_N.B22
91	ODD12_P.B21	1	92	EVN12_P.D21
93	ODD12_N.A21	1	94	EVN12_N.C21
95	ODD13_P.B20	1	96	EVN13_P.G18
97	ODD13_N.A20	1	98	EVN13_N.F18

Pin	Signal	FPGA Bank	Pin	Signal
99	ODD14_P.B19	1	100	EVN14_P.G17
101	ODD14_N.A19	1	102	EVN14_N.F17
103	ODD15_P.F16	1	104	EVN15_P.E17
105	ODD15_N.E16	1	106	EVN15_N.D17
107	GND	1	108	GND
109	ODD16_P.B15	1	110	EVN16_P.F15
111	ODD16_N.A15	1	112	EVN16_N.E15
113	ODD17_P.C14	1	114	EVN17_P.E14
115	ODD17_N.B14	1	116	EVN17_N.D14
117	ODD18_P.A13	0	118	EVN18_P.F13
119	ODD18_N.B13	0	120	EVN18_N.G13
121	ODD19_P.A12	0	122	EVN19_P.C13
123	ODD19_N.B12	0	124	EVN19_N.D13
125	ODD20_P.H13	0	126	EVN20_P.E12
127	ODD20_N.G12	0	128	EVN20_N.F12
129	GND	0	130	GND
131	ODD21_P.F11	0	132	EVN21_P.D11
133	ODD21_N.G11	0	134	EVN21_N.E11
135	ODD22_P.A8	0	136	EVN22_P.C10
137	ODD22_N.B8	0	138	EVN22_N.D10
139	ODD23_P.A7	0	140	EVN23_P.E10
141	ODD23_N.B7	0	142	EVN23_N.F10
143	ODD24_P.D7	0	144	EVN24_P.F9
145	ODD24_N.E7	0	146	EVN24_N.G9
147	ODD25_P.D6	0	148	EVN25_P.B6
149	ODD25_N.E6	0	150	EVN25_N.C6
151	GND	0	152	GND
153	ODD26_P.A4	0	154	EVN26_P.B5
155	ODD26_N.B4	0	156	EVN26_N.C5
157	ODD27_P.D2	7	158	EVN27_P.J5
159	ODD27_N.D1	7	160	EVN27_N.J4
161	ODD28_P.H5	7	162	EVN28_P.H4
163	ODD28_N.J6	7	164	EVN28_N.H3
165	ODD29_P.K6	7	166	EVN29_P.J3
167	ODD29_N.K5	7	168	EVN29_N.J2
169	ODD30_P.G2	7	170	EVN30_P.K4
171	ODD30_N.G1	7	172	EVN30_N.K3
173	GND	7	174	GND
175	ODD31_P.H2	7	176	EVN31_P.L6
177	ODD31_N.H1	7	178	EVN31_N.L5
179	ODD32_P.K2	7	180	EVN32_P.M5
181	ODD32_N.K1	7	182	EVN32_N.M6
183	ODD33_P.L2	7	184	EVN33_P.L4
185	ODD33_N.L1	7	186	EVN33_N.M3
187	ODD34_P.M2	7	188	EVN34_P.N4
189	ODD34_N.M1	7	190	EVN34_N.N3
191	ODD35_P.N2	7	192	EVN35_P.N6
193	ODD35_N.N1	7	194	EVN35_N.N5
195	GND	7	196	GND
197	3.3V	-	198	3.3V

Pin	Signal	FPGA Bank	Pin	Signal
199	3.3V	-	200	3.3V

The signal group description for the above pins is included in Table 2

**Table 2 Signal Group Description**

Signal / Group	I/O	Description
3.3 V	N/A	3.3 volt reference input power referenced to GND.
MRESET#	I	Manual Reset. When pulled to GND for a minimum of 1 usec,
ETH_TD_P / N	O	Ethernet Transmit Data link lines. This pair of signals is from the onboard 10/100 ethernet PHY connected to the DSP EMAC. These pairs should be routed through appropriate 1:1 magnetics prior to exposure to an RJ-45 type connector interface.
ETH_RD_P / N	I	Ethernet Receive Data link lines. This pair of signals is from the onboard 10/100 ethernet PHY connected to the DSP EMAC. These pairs should be routed through appropriate 1:1 magnetics prior to exposure to an RJ-45 type connector interface.
FPGA_RSV1	IO	Reserved, leave disconnected.
FPGA_RSV2	IO	Reserved, leave disconnected.
CLKR0,CLKX0,DR0,DX0,FSR0	IO	These pins are direct connects to the corresponding McBSP port 0 pins on the TMS645x DSP processor. For further interface information, please refer to the TMS645x McBSP Users Guide and Data Sheets.
CLKR1,CLKX1,DR1,DX1,FSR1	IO	These pins are direct connects to the corresponding McBSP port 1 pins on the TMS645x DSP processor. For further interface information, please refer to the TMS645x McBSP Users Guide and Data Sheets.
BOOT_MODE	I	Boot Mode Selection. Reserved for future use. Do not connect.
SCL, SDA	I/O	These pins are direct connects to the I2C interface on the TMS645x DSP processor. For further interface information, please refer to the TMS645x I2C Users Guide and Data Sheets.
GND	N/A	System Digital Ground.
ODDXX_P/N.YYY EVNXX_P/N.YYY	IO	FPGA General Purpose I/O pin. FPGA I/O pins have been routed to the MityDSP connector in pairs denoted ODDXX (odd pin side of connector) or EVNXX (even pin side of connector). When configured for differential termination the pairs

		should be used according to the _P (positive) or _N (negative) extension. The YYY portion of the name corresponds to the FPGA pin location mapped to the signal.
VCCO_N	N/A	FPGA Banks 0, 1, 2, and 7 Voltage configuration. Leave disconnected for 3.3 V bank logic. Connect to 2.5 V for 2.5 volt bank logic (e.g., LVDS). PCB trace must be capable of providing a minimum of 200 mA.

The SO-DIMM-200 also provides the capability to alter the default boot behavior of the DSP according to the table below. For details regarding the various boot modes please refer to the appropriate TI DSP6454 users manuals. Note: use of non-default boot modes is not supported by Critical Link.

### Expansion Interface Description

The Expansion Interface pin-out is described in the table below.

**Table 3 Expansion Interface Pin-Out**

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	PCI_AD16	52	PCI_AD17
3	RIORX0_N	4	RIOTX0_P	53	PCI_AD6	54	PCI_AD18
5	RIORX0_P	6	RIOTX0_N	55	PCI_AD14	56	PCI_STOP#
7	RIORX1_P	8	RIOTX1_P	57	GND	58	PCI_AD26
9	RIORX1_N	10	TIOTX1_N	59	PCI_CLK	50	PCI_AD20
11	RIORX2_N	12	RIOTX2_N	61	GND	62	PCI_CBE2#
13	RIORX2_P	14	RIOTX2_P	63	PCI_AD12	64	PCI_AD24
15	RIORX3_P	16	RIOTX3_N	65	PCI_FRAME#	66	PCI_SERR#
17	RIORX3_N	18	RIOTX3_P	67	PCI_DEVSEL#	68	PCI_RST#
19	RIOCLK125_N	20	GND	69	PCI_PAR	70	PCI_CBE1#
21	RIOCLK125_P	22	HPI_WIDTH	71	PCI_IDSEL	72	PCI_CBE0#
23	GND	24	PCI_AD27	73	PCI_IRDY#	74	PCI_CBE3#
25	PCI_EEAI	26	PCI_AD1	75	PCI_GNT#	76	PCI_REQ#
27	PCI66	28	PCI_AD30	77	PCI_INTA#	78	MAC_SEL
29	PCI_EN	30	PCI_AD0	79	PCI_TRDY#	80	RGMIIL_VREF
31	PCI_AD11	32	PCI_AD4	81	GND	82	GND
33	PCI_AD10	34	PCI_AD22	83	RGMDCLK	84	RGREFCLK
35	PCI_AD3	36	PCI_AD25	85	RGMDIO	86	GND
37	PCI_AD5	38	PCI_AD8	87	RGRXD3	88	RGTXD3
39	PCI_AD29	40	PCI_AD21	99	RGRXD2	90	RGTXD2
41	PCI_AD23	42	PCI_AD13	91	RGRXD1	92	RGTXD1
43	PCI_AD7	44	PCI_AD2	93	RGRXD0	94	RGTXD0
45	PCI_AD9	46	PCI_AD19	95	RGRXCTL	96	RGTXCTL
47	PCI_AD28	48	PCI_AD15	97	RGRXC	98	RGTXC
49	PCI_AD31	50	PCI_ERR#	99	GND	100	GND

### Debug Interface Description

The debug interface connector pin-out is specified in the table below.

**Table 4 Debug Connector Pin-Out**

Pin	Signal	Pin	Signal
1	DSP_EMU0	2	DSP_TMS
3	DSP_EMU1	4	DSP_TDI
5	+3.3V	6	DSP_TDO
7	GND	8	DSP_TCK
9	GND	10	DSP_TRST#
11	FPGA_TDI	12	FPGA_TMS
13	FPGA_TCK	14	FPGA_TDO
15	GND	16	+2.5V

## ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vcc	Voltage supply, 3.3 volt input.			3.3	3.4	Volts
Icc	Quiescent Current draw, 3.3 volt input			1.5	3	Amps
Icc-max	Max current draw, positive 3.3 volt input.			1.7	3.5	Amps
	1. Power utilization of the MityDSP-Pro is heavily dependant on end-user application. Major factors include: CPU PLL configuration, FPGA utilization, and external SDRAM utilization.					

## MECHANICAL INTERFACE

A mechanical outline of the MityDSP-Pro is illustrated in TBS, below.